AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs [0020] and [0021] of the specification as follows:

[0020] The voltage detecting section 30 outputs a reset signal S4 to the CPU 2 when an output voltage Vcc (e.g. Vccl or Vcc2) output by the regulator 10 becomes less than a later mentioned prescribed voltage detection value, set in the voltage detecting section 30. A prescribed voltage detection value may be derived from (Vref x ((r5)/(r4 +r5))) or (Vref x ((r4 + r5)/(r4 + r5 + r6))) ~~(Vref x ((r4 + r5)/r5)) or (Vref x ((r4 + r5 + r6)/(r5 + r6)))~~.

[0021] The control section 20 decreases the prescribed voltage detection value from the first to second level in response to a low level voltage switching signal SI when a power saving mode is set (i.e., when Vcc2 is larger than the second level, and the first level is larger than the Vcc2). The first and second levels correspond to the voltage reference detection values (Vref x ((r4 + r5)/(r4 + r5 + r6))) and (Vref x ((r5)/(r4 +r5))) ~~(Vref x ((r4 + r5 + r6)/(r5 + r6))) and (Vref x ((r4 + r5)/(r5)))~~, respectively. Subsequently, the control section 20 decreases voltage Vcc, output from the regulator 10, down to Vcc2 from Vcc1. Further, when the low level voltage switching signal SI is stopped for the purpose of terminating the power saving mode, the control section 20 synchronously controls the regulator 10 to recover the output voltage Vcc1, and after that controls the voltage detecting section 30 to recover the first voltage level.